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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/066,150	10/26/2001	Hung T. Nguyen	01-621	3566

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EXAMINER	
MEONSKE, TONIA L	
ART UNIT	**PAPER NUMBER**
2181	

DATE MAILED: 12/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/066,150	NGUYEN, HUNG T.	
	Examiner	Art Unit	
	Tonia L. Meonske	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 3, 6, 7, 8, 10, 13, 14, 15, 17, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Leung et al, US Patent 5,784,603, in view of Arizono US Patent 4,910,664.

3. Claims 2, 9, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Leung et al, US Patent 5,784,603, in view of Arizono US Patent 4,910,664, and Bogin et al., US Patent 5,835,435.

4. Claims 4, 11, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Leung et al, US Patent 5,784,603, in view of Arizono US Patent 4,910,664, and Chi, US Patent 6,243,807.

5. Claims 5, 12, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Leung et al, US Patent 5,784,603, in view of Arizono US Patent 4,910,664, and Tokuume, US Patent 4,965,722.

6. The rejections are respectfully maintained and incorporated by reference as set forth in the last office action, mailed on December 10, 2004.

Response to Arguments

7. Applicant's arguments filed September 27, 2005 have been fully considered but they are not persuasive.

8. On pages 6 and 7, Applicant argues in essence:

"Arizono does not prevent the prefetch circuitry from prefetching instructions "outside of said loop until said loop completes execution," and said Arizono fails to teach this limitation."

However, Applicant is directed to Figure 5 of Arizono, and the corresponding description in column 5, line 40-column 45. When all bits of the loop end address register coincide with the prefetch counter, the prefetch counter is reset to the beginning of the loop and no wasteful prefetches are performed (S1 to S2 to S3 to S1). When all bits of the loop end address register, except the LSB, coincide with the prefetch counter, the prefetch counter is reset to the beginning of the loop and one wasteful prefetch is performed into the prefetch que, which is casted away (S1 to S2 to S3 to S4 to S1). Therefore, Arizono has in fact taught *preventing the prefetch circuitry from prefetching instructions outside of said loop until said loop completes execution* (Figure 5, column 5, line 40-column 45, When all bits of the loop end address register coincide with the prefetch counter, instructions outside of the loop are prevented from being prefetched and executed until the loop completes execution.). Therefore this argument is moot.

9. On pages 8-9, Applicant argues in essence:

"There is no motivation to combine Leung and Arizono. ... While both Leung and Arizono are generally directed to computational hardware, the nature of the problems to be solved in each reference is otherwise unrelated. One of ordinary skill in the art attempting to further improve the efficiency of the apparatus of Leung would not look to Arizono for a solution"

However, Leung and Arizono are in fact related references solving the similar problem of speeding up execution time of instructions. Leung recognizes the desirability of achieving high performance standards in a processor (Leung, Columns 1-3). One way Leung increases the performance of the instructions in the processor is by quickly handling mispredicted branch instructions (Leung, abstract). Leung also prefetches instructions to speed up overall instruction execution time. Loops are very common in instruction codes. Arizono proposes a way to reduce the loop processing time while reducing wasteful prefetches (Arizono, columns 5 and 6). Both Arizono and Leung are solving the same problem, speeding up the overall execution time of instructions, so that instructions are executed more efficiently. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the processor of Leung, include the claimed loop recognizer, as taught by Arizono, for the desirable purpose of avoiding wasteful prefetches and reducing the overall processing time of loop instructions. Therefore this argument is moot.

10. On pages 9 and 10, Applicant argues in essence:

"The Applicant's argument that this element provides for "the specific reinstatement of the validity of instructions residing in the instruction cache to obviate the need to fetch these instructions again" (Applicant's Response, March 17, 2005, at paragraph 8) does not argue a limitation not already present in the Claim."

However, Applicant is arguing elements not in the claims. For example, claim 1 claims "a loop recognizer ... reinstates a validity of said fetched instructions in said loop and prevents said prefetch circuitry from prefetching instructions outside of said loop until said loop completes execution". This limitation is entirely different from *"the specific reinstatement of the validity of instructions residing in the instruction cache to obviate*

the need to fetch these instructions again" (emphasis added via underlining). The underlined portions of the argument are not in any of claims 1, 8, and 15. Therefore this argument is moot.

Conclusion

11. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

12. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tonia L. Meonske whose telephone number is (571) 272-4170. The examiner can normally be reached on Monday-Friday, with every other Friday off.

14. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie P. Chan can be reached on (571) 272-4083. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

15. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

tlm

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